**FAST NUCES, Karachi**

Grand Quiz Spring 2018 DLD (EE 227)

Roll No: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_ Total Points: 14 (2 x 7)

Q. No. 1 a) Determine the functional behavior of the circuit in the following Figure 1. Assume that input *C* is driven by a square wave signal.

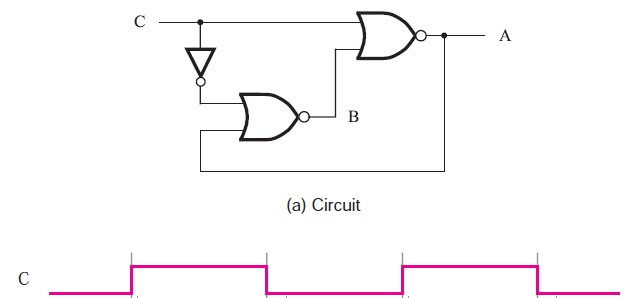


Figure 1

b) For a gated S-R latch, determine the Q and Q outputs for the inputs in Figure 2. Show them in proper relation to the enable input. Assume that Q starts LOW.

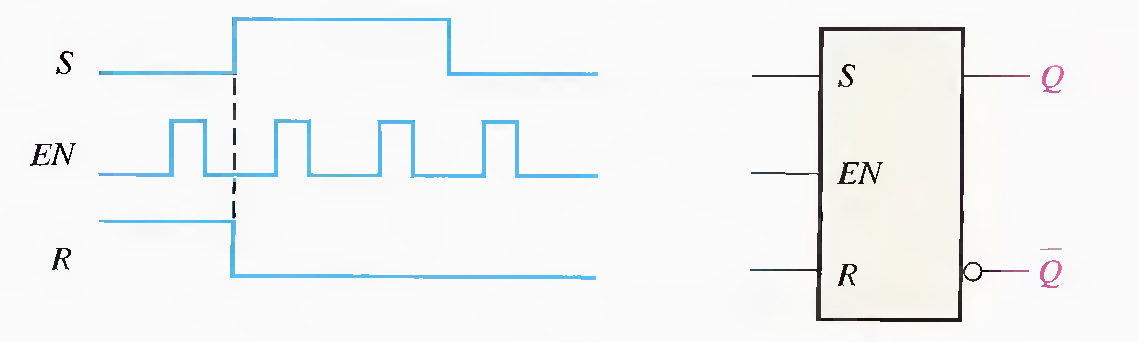


Figure 2

c) Determine the sequence of the counter in Figure 3

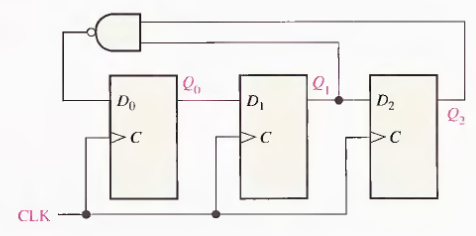


Figure 3

Q. No. 2 a) Implement a full adder circuit by using 3 – to - 8-line Decoder.

b) Implement the logic function in table by using an 8-line data selector/multiplexer.

X(A3, A2, A1, A0) = ∑(2,3,4,8,9,10,11,15)

c) Typically, a manufacturer's data sheet specifies four different propagation delay times associated with a flip-flop. Name and describe each one.

d) Fill the missing values of the 8-to-3 bit priority encoder in the following truth table, where X equals “dont care”, that is logic “0” or a logic “1”.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Digital Inputs | | | | | | | | Binary Output | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Q2 | Q1 | Q0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | **1** | X | 0 | 0 | 1 |
|  |  |  |  |  |  |  |  | 0 | 1 | 0 |
|  |  |  |  |  |  |  |  | 0 | 1 | 1 |
|  |  |  |  |  |  |  |  | 1 | 0 | 0 |
|  |  |  |  |  |  |  |  | 1 | 0 | 1 |
|  |  |  |  |  |  |  |  | 1 | 1 | 0 |
|  |  |  |  |  |  |  |  | 1 | 1 | 1 |